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To the Commissioner of Patents and Trademarks:

Your petitioner, Vladimir VAGANOV, a citizen of the former Soviet Union, and now stateless, and a resident of California, whose post office address is 129 El Porton, Los Gatos, California 95032, prays that letters patent may be granted to him for a

METHOD FOR FABRICATING MICROSTRUCTURES WITH DEEP ANISOTROPIC ETCHING OF THICK SILICON WAFERS

as set forth in the following specification.

METHOD FOR FABRICATING MICROSTRUCTURES WITH DEEP ANISOTROPIC ETCHING OF THICK SILICON WAFERS

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to semiconductor devices, and more specifically to fabrication methods for deep (comparable to the thickness of the semiconductor wafer) etching that do not require expanded device surface areas when scaling up to larger diameter and thicker wafers.

Description of the Prior Art

Various kinds of semiconductor devices micro-sensors, micro-actuators and microstructures require fabricating deep cavities in the monocrystalline silicon substrates. For example, for integrated silicon pressure sensors the initial wafer may be locally etched from the back side through almost the entire thickness to form a thin silicon diaphragm. Similar deep etching (sometimes referred to as bulk micromachining) is used for other sensors and microstructures. For example, piezoresistive accelerometers, ink-jet print-heads, gas sensors, thermopiles, chemical sensors, silicon micro-valves, micro-relays, optical fiber aligners and others use deep silicon etching.

In the fabrication of piezoresistive accelerometers or print heads for ink-jet printers, the surface of an initial silicon wafer may have crystallographic orientation (100). During the fabrication process the wafer is etched locally from the backside to form a silicon diaphragm. Then for the print-head, the nozzles are etched in the diaphragm, or for

the accelerometer the diaphragm is locally etched through to form the required shape of the suspension.

Prior art etching techniques often use wet anisotropic etching. As anisotropic wet etching is a batch process, the productivity is very high and cost is low compared to the other processes for silicon micromachining. Figs. 1(A)-(B) show a cavity 1 formed by wet anisotropic etching of a (100) silicon wafer 2. The shape of the cavity 1 is determined by four {111} planes 3. The etch rate of {111} planes 3 can be several hundred times less than the vertical etch rate of the wafer 2. As a result, the position of the planes 3 remains substantially constant during etching and is determined by the layout of the etching mask and its orientation with respect to the crystallographic directions on the surface of the wafer. In many cases, the etched depth can be well controlled within 0.1-0.5 um with good uniformity across the wafer.

Low cost, high productivity, high accuracy, excellent uniformity and surface quality make wet anisotropic etching a desirable process for deep silicon micromachining. Among some disadvantages of anisotropic etching of (100) orientation silicon is the loss of real estate on the die and wafer surface. As indicated by Figs. 1(A)-(B), the {111} side walls 3 of the etched cavity 1 have about 54 degrees angle to the initial (100) surface of the wafer 2. In order to receive, for example, a square diaphragm 4 with the side one mm, the size of the mask for deep etching to a depth H should be $(1+H\sqrt{2})$mm. A silicon wafer of four inches in diameter usually has a thickness of 0.4 mm. Therefore, the mask for 1 mm diaphragms and for deep (almost through) etching should be 1.56 mm. If the width of the frame around the cavity is 0.47 mm, then the total size of the die will be 2.5 x 2.5 mm and a

four inch wafer will have about 1000 dies. Theoretically, transition to a six inch wafer should result in doubling the number of dies (of the same size) because the area is 2.25 times larger than the area of a four inch wafer. However, the thickness of a six 6 inch wafer is larger and usually equals at least 0.6 mm. Therefore, in order to fabricate the same one mm diaphragm, the mask should be 1.85 mm. With the same width of the frame the size of the die will be 2.79 x 2.79 mm instead of 2.5 x 2.5 mm, resulting in a loss of a minimum of 500 dies on each wafer.

Therefore, there is a need for a process of deep micromachining of silicon wafers which will allow about the same real estate for the mask at the surface of the wafer to form the cavities with different depths and the same size at the bottom (diaphragm). This would allow for decrease in the size of the die and its cost.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a method for decreasing the size and the cost of a die containing microstructures fabricated with deep anisotropic etching using at least a two-step micromachining of monocrystalline silicon wafers.

Another object of the present invention is to provide a method of fabricating cavities with the same size at the bottom (diaphragm) and with an opening mask, which is independent of the initial thickness of the silicon wafer.

Another object of the present invention is to provide a method of micromachining holes through the wafer with the opening mask, which is independent of the initial thickness of the silicon wafer.

Another object of the present invention is to provide a method of micromachining of monocrystalline silicon wafers, which allows fabricating microstructures inside the center of the die and local profiling of the outer surface of the die.

Another object of the present invention is to provide a method for micromachining of bar or grid-like microstructures, which provide additional mechanical strength of the die, and mechanical protection of microstructures inside the cavity, and the protective element and other elements (like diaphragm) can be fabricated within the same wafer and during the same process.

Another object of the present invention is to provide a method for micromachining of bar or grid-like microstructures, which after forming a cavity beneath their structures, can be used as a mask for local etching at the bottom of the cavity.

Another object of the present invention is to provide a method of fabricating channels and cavities completely inside a monocrystalline silicon wafer wherein these channels and cavities can be connected to the surface of the wafer in certain locations and can be used, for example, in microfluidics.

Another object of the present invention is to provide a method of fabricating sealed cavities or channels inside a monocrystalline silicon wafer, for example, for use as for absolute pressure sensors.

A preferred embodiment of the silicon wafer micromachining of the present invention comprises a combination of other than anisotropic deep etching of silicon wafers followed by deep anisotropic etching. The additional etching or deposition of different materials allows fabricating various microstructures for numerous applications.

Brief Description of the Drawings

Figs. 1(A)-(B) are top and side cross-sectional views of a monocrystalline silicon wafer with a pyramidal cavity micromachined therein by wet anisotropic etching of the prior art.

Figs. 2(A)-(D) are side cross-sectional diagrams illustrating cavities etched in a silicon wafer and representing a series of processing steps in a method according to a first embodiment of the present invention.

Figs. 3(A)-(E) are side cross-sectional diagrams illustrating cavities etched in a silicon wafer and representing a series of processing steps in a method according to a second embodiment of the present invention.

Figs. 4(A)-(E) are cross-sectional diagrams illustrating cavities etched in a silicon wafer and representing a series of processing steps in a method according to a third embodiment of the present invention.

Figs. 5(A)-(E) are cross-sectional diagrams illustrating cavities etched in a silicon wafer and representing a series of processing steps in a method according to the fourth embodiment of the present invention.

Figs. 6(A)-(E) are cross-sectional diagrams illustrating cavities etched in a silicon wafer and representing a series of processing steps in a method according to the fifth embodiment of the present invention.

Figs. 7(A)-(C) are cross-sectional diagrams illustrating cavities etched in a silicon wafer and representing a series of processing steps in a method according to the sixth embodiment of the present invention.

Figs. 8(A)-(H) illustrate a summary of options of fabricating various microstructure profiles with the methods described in the illustrated embodiments.

Fig. 9(A) represents a prior art structure of a silicon absolute pressure sensor.

Fig. 9(B) represents structure of a silicon absolute pressure sensor die fabricating from a microstructure according to the present invention.

Figs. 10(A)-(E) are cross-sectional diagrams illustrating enclosed cavities and channels fabricated in a silicon wafer according to the present invention.

Figs. 11(A)-(D) and 15(A)-(F) illustrate enclosed structures fabricated in a silicon wafer according to the present invention.

Figs. 12(A)-(F) illustrate enclosed structure fabricated in silicon wafer according to the present invention.

Figs. 13(A)-(B) are perspective view of microstructures fabricated according to methods of the present invention.

Figs. 14(A)-(B) are perspective view of microstructures fabricated according to methods of the present invention.

Figs. 15(A)-(C) illustrate further structures fabricated in a silicon wafer according to the present invention.

Figs. 16(A)-(L) are cross-sectional diagrams of micromechanical structures fabricated with the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The drawings illustrate various profiles, which can be obtained by employing a combination of deep anisotropic etching with at least one other type of etching. A detailed description of the process according to the present invention,

which can be used for forming such profiles is provided hereafter in the following description of the various embodiments.

Referring to the embodiment of Figs. 2(A)-(D), a cross-section of a silicon wafer 12 is shown in Fig. 2(A). Before micromachining, the wafer 12 has uniform thickness. A protective mask layer 13 is formed on at least one side of the wafer 12 as shown in Fig. 2(B). An opening 14 in the mask layer 13 is defined by one of the known techniques, for example, by photolithography. The protective mask layer may contain silicon dioxide, silicon nitride, silicon carbide, photoresist, polyimide or metal.

The first step of the micromachining process is a local RIE (reactive ion etching) or other etching method, which allows for a cavity 15 profile with vertical walls. The term "vertical" herein means that the angle between the side wall of the cavity 15 and the top surface of the wafer is approximately 90°, although it can be slightly smaller or larger than 90° depending on the process. Commercially available are equipment and processes which provide for the formation of cavities with vertical walls in monocrystalline silicon wafers. In order to simplify the description, this step is referred to as the RIE step or as first RIE step.

Micromachining of the silicon wafer 12 can be continued after the RIE step using wet anisotropic etching. Well-known in the art, etchants such as potassium hydroxide (KOH), alkali metal hydroxides, tetramethyl-ammonium hydroxide, ethylenediamine, gallic acid or hydrazine can be used at this step. The profile shown in Fig. 2(D) can be obtained after wet anisotropic etching. The shape of the cavity is determined by {111} planes 16. Position of the bottom plane

determines both thickness and size of a diaphragm 17. To further expedite, the anisotropic etching can be performed in the presence of ultrasonic or megasonic vibrations in the etching solution.

To illustrate the benefit of the initial RIE step, if anisotropic etching were used without the first RIE step with the opening 14 of the initial size, then the shape of the cavity would be determined by {111} planes 18a and intersect above the surface of diaphragm 17. As illustrated by 2(D), the diaphragm 17 with the same thickness as that formed with the combined RIE and wet anisotropic etching cannot be obtained by the wet anisotropic etching only and using the initial size opening 14. The combination of RIE and wet anisotropic etching allows for increasing the surface size of the diaphragm 17 and decreasing the thickness of the diaphragm without altering the size of the wafer die. In order to get the same size of the diaphragm 17 using wet anisotropic etching only, it would be necessary to use larger size of the initial opening 14 as illustrated by the broken line planes 18b. As illustrated by Fig. 2(D), for a given size of diaphragm 17 the combination of RIE and wet anisotropic etching provides for decreasing the size of the initial opening 14 for micromachining and, consequently, die size decreasing.

In the processing according to a second embodiment, as illustrated in Figs. 3(A)-3(E), the initial etch step is a local RIE etch, which is performed as described in the first embodiment. Then the surface of the cavity 15 and layers 13 are covered with a mask layer 21 as shown in Fig. 3(C). For example, the layer 21 can be done by thermal oxidation, or LPCVD, or PECVD oxide/nitride deposition. The mask layer 21

is then removed from the bottom of cavity 15 as shown in Fig. 3(D). Wet anisotropic etching at the next step then provides formation of the profile shown in Fig. 3(E). The position of the bottom plane determines both thickness and size of a diaphragm 26. If anisotropic etching were used without the RIE, masking and mask removal steps and the size of the initial opening 14 remained the same, then the shape of the cavity would be determined as illustrated by the broken line planes 28a. Again, the planes 28a intersect considerable above and therefore the diaphragm surface area is smaller and the diaphragm is thicker. As illustrated in Fig. 3(E), a diaphragm with the same thickness as that formed with the combined RIE and wet anisotropic etching cannot be obtained by the wet anisotropic etching only and using the initial size of the opening 14. However, the combination of RIE and wet anisotropic etching allows increasing the size of the diaphragm for the same size of wafer die. To realize the same size of diaphragm using wet anisotropic etching only, necessitates use of a larger size initial opening 14 with the shape of the cavity being determined as illustrated by planes 28b. As illustrated in Fig. 3(E), for the same size of diaphragm the combination of RIE and wet anisotropic etching allows for die size decreasing.

As illustrated in Figs. 4(A)-(E), in the process according to a third embodiment, the major initial steps are after masking off the wafer 12, and forming the opening 14 in the mask 13 as in Fig. 2(A)-(B) are as follows: (a) local RIE etch to form cavity 15 (see Fig. 4(A)); (b) masking the side walls and bottom plane of the cavity 15 (see Fig. 4(B)); and (c) removing mask 21 from the bottom plane of the cavity (see Fig. 4(C)). These steps are performed as previously described

in the second embodiment (see Figs. 3(B)-3(D). Then, a second silicon etch step, which allows for forming a deeper cavity 15 profile with the vertical walls. The second silicon etch step can be performed by the same process as the first wafer etch step, or a different process can be used. To simplify the description, this step is referred to as the second RIE step. The profile of the cavity 15 after the second RIE step is shown in Fig. 4(D). The side walls of the cavity 15 remain vertical. The difference between profiles shown in Fig. 2(C) and Fig. 4(D) is that in the Fig. 2(C) profile the side walls of the cavity 15 are not covered with the mask layer 21. In the Fig. 4(D) profile, side walls of the cavity 15 are partially covered by the mask 21. Wet anisotropic etching is then used at the next step and the profile of the cavity after wet anisotropic etching is shown in Fig. 4(E).

If anisotropic etching were used without the above described RIE steps and the initial opening was of the same size, then the shape of the cavity would be determined by {111} planes 38a. As it can be seen from Fig. 4(E), a diaphragm with the same thickness as that formed with the combined RIE and wet anisotropic etching cannot be obtained by the wet anisotropic etching only using the initial size of the opening 14. The combination of RIE and wet anisotropic etching steps allow increasing size of the diaphragm 26 for the same size of the die. In order to get the same size of the diaphragm 26 using wet anisotropic etching only it is necessary to use a larger initial opening 14. When the size of the opening 14 is larger, then the shape of the cavity is still determined by the illustrated broken line planes 38b. As illustrated by Fig. 4(E), for the same size of the diaphragm 26, the combination of RIE and wet anisotropic etching allows for a

decreased size of initial opening 14. The smaller size initial opening 14 allows for decreased size of wafer die.

As illustrated in Figs. 5(A)-5(E), the process according to a fourth embodiment includes major initial steps of masking of the wafer 12 and forming the opening 14 in the mask 13 followed by: (a) local RIE etch (see Fig. 5(A)); (b) masking the side walls and bottom plane of the cavity 15 (see Fig. 5(B)); (c) removing mask 21 from the bottom plane of the cavity 15 (see Fig. 5(C)).

Isotropic etching then is used at the next step. Well-known in the art, etchants of a mixture of hydrofluoric (HF), nitric (HNO_2) and acetic (CH_3COOH) acids, or SF_6 plasma etch, or atmospheric downstream plasma (ADP) etch, or gas xenon difluoride can be used at this isotropic etch step. The profile of the cavity 15 after isotropic etching is shown in Fig. 5(D). Wet anisotropic etching is then used in the next step and the profile of the cavity is shown in Fig. 4(E). The advantage of the isotropic etch step is that the size of the diaphragm can be increased relative to that in the case of using wet anisotropic etch after the second RIE etch. To get the same size of the diaphragm 26 using wet anisotropic etch requires a larger initial opening 14. As evident from Fig. 5(E), for the same size diaphragm 26, the combination of RIE isotropic and anisotropic etching allows for decreased size of the initial opening 14, which in turn allows decreasing the size of the wafer die.

As illustrated in Figs. 6(A)-6(E), the process according to the fifth embodiment includes the major initial steps of masking of the wafer 12, and forming the opening 14 in the mask 12, followed by: (a)local RIE etch (see Fig. 6(A)); (b) masking the side walls and bottom plane of the cavity 15 and

removing mask 13 from the bottom plane of the cavity 15 (see Fig. 6(B); (c) local RIE etch (see Fig. 6(C)); (d) isotropic etch (see Fig. 6(D)); and (e) wet anisotropic etch (see Fig. 6(E)).

The anisotropic etch step provides for forming the diaphragm with better defined edges and with more uniform thickness than the isotropic etch does. Wet anisotropic etching also allows better cavity depth control. Therefore, combination of isotropic and anisotropic etching allows increasing size of the diaphragm 26 for the same size of the opening 14 and good control of diaphragm 26 thickness.

In order to realize the same size of the diaphragm 26 using wet anisotropic etching only it is necessary to use larger size of the initial opening 14. As illustrated by Fig. 6H, for the same size diaphragm 26 the combination of RIE, isotropic, and anisotropic etching allows decreasing the size of the initial opening 14 and decreasing the size of the wafer die.

As illustrated in Figs. 7(A)-7(C), the process according the sixth embodiment includes the major initial steps of masking of the wafer 12, forming an opening 14 in the mask 13, local RIE etch, masking of the side walls and bottom plane of the cavity 15, removing mask 21 from the bottom plane of the cavity 15, followed by: (a) isotropic etch (see Fig. 7(A)); (b) wet anisotropic etch (see Fig. 7(B)); and (c) a second isotropic etch (see Fig. 7(C)).

The cavity 15, after wet anisotropic etching, as shown in Figs. 6(E) and 7(C) typically has well defined edges and corners. When a profiled structure with such a cavity is mechanically loaded by a force and/or a torque then the induced mechanical stress tends to concentrate in the edge

areas and corner areas. This induced stress can be deleterious to the mechanical structure and the wafer. The second isotropic etching provides rounding of corners and edges of the cavity 15 thereby improving mechanical properties of the structure and preventing cracking of the wafer 12.

The preceding described processes for profiling semiconductor wafers using multiple etch steps are summarized by Fig. 8(A)-(H). These processes can be used for creating complex micromechanical structures on semiconductor wafers.

The microstructures containing closed cavities and/or channels have various applications. For example, microstructure with a closed cavity and channels can be used in an absolute pressure sensor. A form of a prior art structure of an absolute pressure sensor 100 is shown in Fig. 9(A). In the structure 100, a cavity 102 in a silicon die 104 is formed using wet anisotropic etching to create a diaphragm 105. After that, the silicon die 104 is bonded with a second die 106. The second die 106 can be made of, for example, glass or silicon. In the absolute pressure sensor 100, the connection of the die 104 with the second die 106 is formed with an intermediate bonding layer 108. Frit glass can be used, for example, as the intermediate 108, which provides hermetic sealing of the cavity 102.

An absolute pressure sensor die 200 utilizing the method of the present invention is shown in Fig. 9(B). The absolute pressure sensor die 200 includes a cavity 202 in a silicon die 204 to form a diaphragm 205 with a sealing material 206 of glass, polycrystalline silicon, etc., adhered with an intermediate layer 208 and sealing channels 232. Absolute pressure sensors 200 per the present invention have several advantages in comparison with the absolute pressure sensors of

the prior art. First, for the same size die the size of the diaphragm is larger, or for the same size of the diaphragm, the silicon die fabricated according to the present invention has smaller size. Besides, it is thinner, because it requires only one wafer instead of two in the prior art.

As described the method for fabricating microstructures allows for direct formation of microstructures with channels. Such microstructures can be used in applications where forming of micro-capillaries is necessary. For example, such microstructures with internal channels can be used in micro-systems for DNA analysis and blood analysis as well as in fluidic sensors. Structures pursuant to the present invention provide several advantages. First, for the same linear dimension of the die, it allows formation of micro-channels with larger cross-sectional areas than that which can be formed by wet anisotropic etching. Second, there is no need for a second die (for example, made of glass or silicon), as is typically used to form closed channels. Third, the cross-section of the channel can be controlled with accuracy when it is determined by {111} planes only.

The profile shown in Fig. 10(A) can be formed on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming a set of openings in the mask 13; (c) RIE etching through said set of openings forming cavities with vertical walls; (d) masking the side walls and bottom plane of said cavities; (e) removing mask from the bottom plane of the outermost cavities; and (f) wet anisotropic etching. Then the layer 206 is deposited.

The profile of Fig. 10(B) can be formed on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming a set of openings in the mask 13; (c) RIE etching

through said set of openings forming cavities with vertical walls; (d) masking of the side walls and bottom plane of the cavities; (e) removing mask 21 from the bottom plane of the outermost cavities; (f) a second RIE etching to deepen the outer cavities; (g) wet isotropic etching; and (h) depositing sealing layer 206.

The profile of Fig. 10(C) can be formed on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming an opening in the mask 13; (c) RIE etching through the opening forming a cavity with vertical walls; (d) masking the side walls and bottom plane of the cavity; (e) removing mask 21 from the bottom plane of the cavity; (f) second RIE etching to deepen the cavity; (g) wet isotropic etching; and (h) depositing sealing layer 206.

The profile of Fig. 10(D) can be formed on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming an opening in the mask 13; (c) RIE etching through said opening forming a cavity with vertical walls; (d) masking the side walls and bottom of the cavity; (e) removing the mask from the bottom of the cavity; (f) wet anisotropic; (g) masking; (h) removing mask from inverting walls; (i) RIE etching to form vertical walls extending from the outward extending walls; (j) masking; (k) removing mask from bottom of the cavity; (l) wet anisotropic; and (m) depositing sealing layer 206.

The profile of Fig. 10(E) can be formed on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming an opening in the mask 13; (c) RIE etching through said opening forming a cavity with vertical walls; (d) masking the side walls and bottom of the cavity; (e) removing the mask from the bottom of the cavity; (f) wet anisotropic; (g)

masking; (h) removing mask from bottom-most inverting walls; (i) RIE etching to form vertical walls extending from the outward extending walls; (j) masking; (k) remove mask from bottom of the cavity; (l) wet anisotropic; (m) isotropic etching; and (n) sealing layer 206.

The profile shown in Fig. 11(D) can be formed on silicon wafer 12 (Fig. 11(A)) with the following process: (a) masking the wafer 12; (b) forming a set of openings 14 in the mask 13 (Fig. 11(A)); (c) RIE etching through said set of openings forming cavities with vertical walls (Fig. 11(B));(d) wet anisotropic etching (Fig. 11(C)); and (e) depositing sealing layer 206 (Fig. 11(E)).

The profile shown in Fig. 12(F) can be formed on silicon wafer 12 with the following process: (a) masking the wafer 12; (b) forming a set of openings 14 in the mask 13; (c) RIE etching through said set of openings forming cavities with vertical walls (Fig. 12(A)); (d) masking the side walls and bottom plane of said set of openings (Fig. 12(B)); (e) removing mask from the bottom plane of the cavities (Fig. 12(C)); (f) RIE etching to extend the cavities with vertical walls (Fig. 12(D)); (g) anisotropic etching (Fig. 12(E)); and (h) depositing sealing layer 206 (Fig. 12(F)).

Figs. 13(A)-13(B) and 14(A)-14(B) illustrate microstructures 400, 500, 600 and 700, respectively, formed according to the method described in the present invention. These structures each contain a cavity and a grid structure formed on the surface of a silicon wafer. The bars of a grid structure can be oriented differently with respect to the side walls of the cavity depending on the masking.

The microstructure 400 of Fig. 13(A) has openings 402 with sides oriented parallel to the crystallographic

directions {100} at the surface of a silicon wafer 404. Bars 406 of the grid are at a 45° an angle relative to the crystallographic direction {110}.

The microstructure 500 shown in Fig. 13(B) has openings 502 with sides oriented parallel to the crystallographic directions {110} at the surface of a silicon wafer 504. Bars 506 of the grid are parallel to the same crystallographic direction.

In the microstructures 600 and 700 in Fig. 14(A) and 14(B), the openings are holes of different shape and different layout dependent on the masking pattern.

The grid structure shown in Fig. 11,12, 13 and can perform various functions. Such a structure protects the cavity from particles, increases mechanical strength of the profiled silicon die and profiled silicon wafer, which reduces mechanical breakage of profiled silicon wafers and increases mechanical overload limits to the die. Functional elements can be fabricated within the bars, which form the grid. For example, a heater can be formed in the bars. Such a heater allows decreasing time of heating a gas or liquid in the cavity. The same structure can increase heat transfer from the cavity, i.e. can be used as a heat exchanger.

Another application of the bars or grids is that they can be used as a mask for additional etching of the bottom surface of the cavity, as shown in Fig. 15. After forming a grid with the openings 232 and cavity 202, as shown in Fig. 15(A), the bottom of the cavity can be additionally locally etched through the openings 232 by RIE etch to form channels 210. The grid or bars serve as a mask during this process. After that, the openings 232 are sealed, as shown in Fig. 15(B) with sealing layer 206. Additional local etching at the bottom of

the cavity 202 forms through holes 212 in the diaphragm 205, as shown in Fig. 15(B). In a further version of this process, a layer 220 is deposited over the bottom surface of die 204 with inlets, outlets, nozzles 216 aligned with and through holes 212. This kind of structure can be useful in different microfluidic devices.

Figs. 16(A)-16(L) show twelve different cross-sections of the micromechanical structures formed with multiple etch steps according to the present invention. Although such profiles can be useful in different applications, they are discussed herein regarding the die outer shape and shape of the cavity formed within said die. Each cross-section shown in Figs. 16(A)-16(L) is a die cross-section, which can be obtained after wafer separation. The profile formed along die separation lines can be reconstructed assuming that the shown cross-section is a cell in a periodic structure.

Fig. 16(A) shows a profile, which can be obtained on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming a first and a second set of openings in the mask 13; said first set of openings is used for etching cavities 15 located inside the die; said second set of openings is used for etching cavities between the dies; (c) RIE etching through said first and second sets of openings to form cavities with vertical walls followed by; (d) wet anisotropic etch.

The openings for etching cavities between the dies are narrower than that for etching cavities inside the die. Because of that, said wet anisotropic etching allows forming diaphragms or through holes inside the die 12, and self-stop grooves 300, which shape is determined by {111} planes, are formed between the dies 12.

Fig. 16(B) shows a profile, which can be obtained on silicon wafers with the following process: (a) masking of the wafer 12; (b) forming a first and a second set of openings in the mask 13; said first set of openings is used for etching cavities located inside the die; said second set of openings is used for etching cavities between the dies; (c) RIE etching through said first set of openings to form cavities with vertical walls, the second set of openings is protected during this step, for example by photoresist; and then (d) wet anisotropic etch. After wet anisotropic etching dies 12 are separated by V-grooves 302 (self-stop profile), which shape is determined by {111} planes. The diaphragm 26 or a through hole is formed within each die.

Fig. 16(C) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first and a second set of openings in the mask; said first set of openings is used for etching cavities located inside the die 12; the second set of openings is used for etching cavities between the dies; (c) RIE etching through said first and second sets of openings to form cavities with vertical walls; (d) masking of the side walls and bottom planes of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; (f) removing mask both from the side walls and bottom plane of the second set of the cavities; and then (g) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die 12, closed channels 32 are formed and dies 12 are separated by grooves 306 of self-stop profile, which shape is determined by {111} planes.

Fig. 16(D) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of

the wafer 12; (b) forming a first and a second set of openings in the mask 13 with said first set of openings for etching cavities located inside the die and said second set of openings for etching cavities between the dies 12; (c) RIE etching through said first and second set of openings to form cavities with the vertical walls; (d) masking the side walls and bottom planes of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; and then (f) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die. Dies 12 are separated by U-grooves 308 with vertical walls.

Fig. 16(E) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first set of openings in the mask 13, said first set of openings for etching cavities located inside the die; (c) RIE etching through said first set of openings to form cavities with vertical walls; (d) masking of the side walls and bottom plane of the cavities; (e) removing mask 21 from the bottom plane of the first set of the cavities; (f) forming a second set of openings in a mask for etching cavities between the dies; (g) RIE etching through said first and second sets of openings to form cavities with vertical walls which are etched through the first set of openings and deepened and cavities with vertical walls through the second set of the openings; and then (h) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die and dies are separated by the grooves 306 with self-stop profile determined by {111} planes.

Fig. 16(F) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of

the wafer 12; (b) forming a first set of openings in the mask 13; said first set of mask openings is used for etching cavities located inside the die 12; (c) RIE etching through said first set of mask openings to form cavities with the vertical walls; (d) masking of the side walls and bottom plane of the cavities; (e) removing mask 21 from the bottom plane of the first set of the cavities; (f) RIE etching through said first set of mask openings such that cavities with vertical walls are deepened; (g) forming a second set of mask openings for etching cavities between the dies 12; and then (h) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die and dies are separated by the V-grooves 302 with self-stop profile determined by the {111} planes.

Fig. 16(G) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first set of openings in the mask for etching cavities located inside the die 12; (c) RIE etching through said first set of mask openings to form cavities with the vertical walls; (d) masking the side walls and bottom plane of the cavities; (e) removing mask 21 from the bottom plane of the first set of the cavities; (f) forming a second set of mask for etching cavities between the dies 12; (g) RIE etching through said first and second sets of openings to form cavities with vertical walls with the cavities etched in step (c) deepened; and then (h) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die and the dies 12 are separated by circular grooves 310.

Fig. 16(H) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of

the wafer 12; (b) forming a first and second set of openings in the mask 13 with the first set of mask openings for etching cavities located inside the die 12 and the second set of mask openings for etching cavities between the dies 12; (c) RIE etching through said first and second set of mask openings to form cavities with the vertical walls; (d) masking of the side walls and bottom plane of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; (f) first isotropic etching such that said first set of cavities is deepened; (g) removing mask from the side walls and bottom plane of the second set of the cavities; and then (h) second isotropic etching. After second isotropic etching, the diaphragm 26 or through hole is formed within each die 12. Dies are separated by the U-grooves 312 with vertical walls and rounded edges.

Fig. 16(I) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first set of openings in the mask 13 for etching cavities located inside the die; (c) RIE etching through said first set of mask openings to form cavities with the vertical walls; (d) masking the side walls and bottom plane of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; (f) forming a second set of mask openings for etching cavities between the dies; (g) RIE etching through said first and second sets of mask openings to form cavities with vertical walls with the cavities etched in step (c) deepened; and then (h) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die 12. Dies are separated by the grooves 306 with self-stop profile determined by {111} planes.

Fig. 16(J) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first set of openings in the mask 13 for etching cavities located inside the die; (c) RIE etching through said first set of mask openings to form cavities with the vertical walls; (d) masking of the side walls and bottom plane of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; (f) RIE etching through said first set of mask openings to form vertical walls; (g) isotropic etching; (h) forming a second set of mask openings for etching cavities between the dies 12; and then (i) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die 12 and dies are separated by the V-grooves 302 with self-stop profile determined by {111} planes.

Fig. 16(K) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first set of openings in the mask 13 for etching cavities located inside the die; (c) RIE etching through said first set of mask openings to form cavities with the vertical walls; (d) masking the side walls and bottom plane of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; (f) forming a second set of mask openings for etching cavities between the dies; (g) RIE etching through said first and second sets of openings to form cavities with vertical walls with the cavities etched in step (c) deepened; (h) first isotropic etch step; (i) wet anisotropic etching; and then (j) second isotropic etch step. After second isotropic etching, the diaphragm 26 or through hole is formed within each die. Dies are separated by grooves 314, which are obtained by

combination of the four etch steps: RIE, first isotropic etching, wet anisotropic etching, and second isotropic etching.

Fig. 16(L) shows a profile, which can be obtained on a silicon wafer 12 with the following process: (a) masking of the wafer 12; (b) forming a first set of openings in the mask 13 for etching cavities located inside the die; (c) RIE etching through said first set of openings to form cavities with vertical walls; (d) masking the side walls and bottom plane of the cavities; (e) removing mask from the bottom plane of the first set of the cavities; (f) RIE etching through said first set of mask openings to form deepened cavities with the vertical walls; (g) isotropic etching; (h) forming a second set of mask openings for etching cavities between the dies 12; and then (i) wet anisotropic etching. After wet anisotropic etching, the diaphragm 26 or through hole is formed within each die and dies are separated by the grooves profile 316, which is determined by combination of wet anisotropic and isotropic etching.

It should be understood that variations of the process and geometry of microstructures, which can be formed according to the present invention, and which were described in the preferred embodiments do not limit the present invention, but only illustrate some of the various technical solutions covered by this invention.